

KL5C80A12



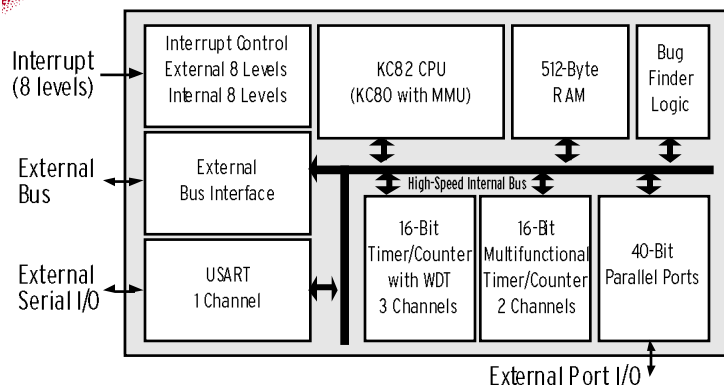
FEATURES

- **CPU core:** KC80 (external 8-bit data bus internal 16-bit data path)
 - **Instruction Set:** Fully compatible with Z80 MPU at binary level
 - **High speed operation:** 10 MHz, 4 times faster than Z80 at the same clock rate
 - **Operational clock frequency:** 0-10 MHz
 - **Minimum execution time:** 100 nS (1 clock)
 - **Address space:** 512-Kbyte
 - **Timer/counter:** Event, interrupt and interval count, PWM, WDT modes
 - **Interrupt controller:** NMI and internal/external 16 levels of maskable interrupts, nested interrupt support
Mode 2 (vector) interrupt operation
 - **Parallel port:** 1- or 4-bit wise configurable input or output direction
Bit set/reset function
 - **Serial channel:** Full-duplex USART (X1)
Max baud rate 2 Mbps
 - **On chip memory:** 512-byte high speed RAM (no wait accessible)
 - **External bus interface:** External bus interface unit with a wait state controller
 - **Other functions:** Clock generator and debug logic
 - **100-pin QFP package:**
 - **Software debug tool:** Target probe-type ICE, handy type debug tool 'Bug Finder', ROM-ICEs, software debug tools, simulator, and general purpose CPU boards are available from third parties.
- ◆ **Best suited for local controller for various types of embedded system.**
- ◆ **KC80 ASIC microcontrollers are also available. (Various types of peripherals, macro cells and high speed on chip ROM/RAM can be integrated.)**

PERFORMANCE COMPARISON

Instructions	KL5C80A12	Z80
LD B, C	1 clock	4 clocks
ADD HL, BC	1 clock	11 clocks
DEC DE	1 clock	6 clocks
POP AF	3 clocks	10 clocks
JR Z, +20h	3 clocks	12 clocks

INTERNAL BLOCK DIAGRAM



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